AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application.

Listings of Claims:

1. (Currently Amended) A method, comprising:

transferring a data block between a flash memory and a memory controller; ~~and~~

computing an ECC for said data block while transferring the data block; and

selectively storing the ECC in a plurality of registers using a switching mechanism.

2. (Original) The method of claim 1, wherein transferring the data block comprises transferring the data block between a NAND Flash memory and the memory controller.

3. (Currently Amended) The method of claim 1, ~~further comprising~~ wherein selectively storing the ECC further comprises

storing a first portion of the ECC in a first register; and

storing a second portion of the ECC in a second register if the first register is full.

4. (Currently Amended) The method of claim 3, wherein storing in a second register comprises selecting the second register using ~~a~~ the switching mechanism.

5. (Original) The method of claim 1, wherein computing the ECC comprises performing the exclusive-or function.

6. (Currently Amended) A system, comprising:

a flash memory;

a controller coupled to the flash memory;

a switch coupled to the controller; and

~~wherein~~ said controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block; and

said system is configured to selectively store the ECC in a plurality of registers using the switch.

7. (Original) The system of claim 6, wherein the flash memory is a NAND Flash memory.

8. (Previously Presented) The system of claim 6, wherein the system is configured to

store a first portion of the ECC in a first register; and

store a second portion of the ECC in an alternate register if the first register is full.

9. (Previously Presented) The system of claim 8, wherein the controller is configured to transfer contents of all registers to memory if all registers are full.

10. (Currently Amended) The system of claim 8, ~~further comprising~~wherein ~~a~~ the switch configured to select the alternate register.

11. (Previously Presented) The system of claim 6, wherein the controller is configured to compute the ECC while performing the exclusive-or function.

12. (Currently Amended) A system comprising:

a means for storing a data block;

a means for controlling the data block;

a means for computing an ECC of the data block; ~~and~~

a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block~~.~~; and

a means for selectively storing the ECC in a plurality of registers.

13. (Original) The system of claim 12, wherein the means for storing is a NAND Flash memory.

14. (Currently Amended) The system of claim 12, wherein the ~~system~~ means for selectively storing the ECC is configured to

store the ECC in a first register; and

store the ECC in an alternate register if the first register is full.

15. (Previously Presented) The system of claim 12, wherein the system is configured to transfer contents of at least one register to memory if all registers are full.

16. (Currently Amended) The system of claim 14, ~~further comprising~~ wherein the means for selectively storing the ECC is a switch configured to select the alternate register.

17. (Previously Presented) The system of claim 12, wherein the system is configured to compute the ECC while performing the exclusive-or function.

18. (Currently Amended) A memory controller configured to couple to a memory, comprising:

a memory interface; ~~and~~

an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory.; and

a switching mechanism coupled to the ECC engine, the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism.

19. (Currently Amended) The memory controller of claim 18, further comprising:

~~a switching mechanism coupled to the ECC engine; and~~

a register bank coupled to the switching mechanism, comprising at least one register;

wherein the ECC engine configured to store the ECC in a register selected by the switching mechanism, the register having space available for ECC storage.

20. (Previously Presented) The memory controller of claim 18, wherein the controller is configured to transfer a data block while transferring the data block between the ECC engine and a flash memory.

21. (Previously Presented) The memory controller of claim 18, wherein the controller is configured to transfer a data block while transferring the data block between the ECC engine and a NAND Flash memory.

22. (Previously Presented) The memory controller of claim 18, wherein the ECC engine is configured to transfer a data block by reading the data block from memory.

23. (Previously Presented) The memory controller of claim 18, wherein the ECC engine is configured to transfer a data block by writing the data block to memory.

24. (Previously Presented) The system of claim 8, wherein the first register is in the controller.

25. (Previously Presented) The system of claim 8, wherein the alternate register is in the controller.

26. (Previously Presented) The system of claim 10, wherein the switch is in the controller.